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|--|-------------|----------------------|----------------------|------------------|
| APPLICATION NO.  | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO.  | CONFIRMATION NO. |
| 09/848,642   | 05/03/2001  | Shunpei Yamazaki     | SEL 258              | 7227             |
| 7590                    12/31/2009<br>COOK, ALEX, MCFARRON, MANZO,<br>CUMMINGS & MEHLER, LTD.<br>Suite 2850<br>200 West Adams St.<br>Chicago, IL 60606 |             |                      | EXAMINER             |                  |
|  |             |                      | SCHECHTER, ANDREW M. |                  |
|  |             |                      | ART UNIT             | PAPER NUMBER     |
|  |             |                      | 2883                 |                  |
|  |             |                      | MAIL DATE            | DELIVERY MODE    |
|  |             |                      | 12/31/2009           | PAPER            |

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

|                              |                                      |  |
|------------------------------|--------------------------------------|--|
| <b>Office Action Summary</b> | <b>Application No.</b><br>09/848,642 | <b>Applicant(s)</b><br>YAMAZAKI ET AL. |
|                              | <b>Examiner</b><br>ANDREW SCHECHTER  | <b>Art Unit</b><br>2883                |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
  - If no period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(o).

#### Status

- 1) Responsive to communication(s) filed on 09 September 2009.
- 2a) This action is FINAL.      2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 21-24, 76,77 and 85-102 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) 21-24, 76,77,85-90,93,94,97 and 98 is/are allowed.
- 6) Claim(s) 91,92,95,96,99 and 100 is/are rejected.
- 7) Claim(s) 101 and 102 is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 05 March 2004 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All    b) Some \* c) None of:
1. Certified copies of the priority documents have been received.
  2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO/SB/08)  
 Paper No(s)/Mail Date \_\_\_\_\_
- 4) Interview Summary (PTO-413)  
 Paper No(s)/Mail Date. \_\_\_\_\_
- 5) Notice of Informal Patent Application
- 6) Other: \_\_\_\_\_

**DETAILED ACTION**

***Drawings***

1. The drawings are objected to because on the right-hand side of Fig. 15, element 907 (the fourth insulating layer on top of layer 909) is mislabeled as "906". The label "906" is correctly used in the middle of the figure to indicate the recited second wiring on top of layer 907. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Response to Arguments***

2. Applicant's arguments filed 9 September 2009 have been fully considered but they are not persuasive. Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

The amendments to the claims overcome the previous rejections under 35 USC 112, first paragraph. Claims 101 and 102 are now clearly supported by the applicant's Fig. 15.

The applicant argues [p. 15] that the recited structure of the reverse stagger TFT in amended claims 91 and 92 is not disclosed or suggested by the previously applied references. This is true of *Noguchi*, applied in the office action of 9 June 2009, which has a different TFT structure. However, the amended claims are now similar to those of 2 July 2008, which were rejected on 6 August 2008 relying on the reverse stagger TFT structure disclosed by *Sakamoto*, Japanese Patent Document No. 9-160509. Analogous rejections to those of 6 August 2008 are therefore made below.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 91, 92, 95, 96, 99, and 100 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Sakamoto*, Japanese Patent Document No. 9-160509 (made of

record with a translation by the applicant) in view of *Yokomizu*, Japanese Patent Document No. 10-073813, *Kanemoto et al.*, U.S. Patent No. 5,493,429, and *Yoneya et al.*, U.S. Patent No. 6,300,926.

*Sakamoto* discloses [see Fig. 2, for instance] an electro-optical device comprising a first substrate [20], a reverse stagger type TFT formed over the first substrate comprising a gate electrode [1], a first insulating film [4] formed on said gate electrode, a semiconductor layer [5] having at least a source region [6], a drain region [7], and a channel formation region [between them; note that the labels 'source' and 'drain' are reversed in the reference, though the structure is the same] formed over the first insulating film; a source wiring [2] formed over the first substrate, wherein the source wiring is electrically connected to the source region through a second wiring [12] formed over the first insulating film, and wherein the first insulating film is formed on the source wiring; and a pixel electrode [15] comprising a first transparent conductive film [ITO, see paragraph 0017], and electrically connected to the drain region [via 13], and a liquid crystal [see paragraph 0001].

*Sakamoto* does not necessarily explicitly disclose (at least for this embodiment) a second substrate opposed to the first substrate, at least a first colored layer and a second colored layer formed in the second substrate, partly overlapping each other; an organic resin film covering the first and second colored layer; an opposing electrode comprising a second transparent conductive film; a liquid crystal interposed between the pixel electrode and opposing electrode, wherein the organic resin film is interposed between the liquid crystal and the first and second colored layers and has a thickness of

1  $\mu\text{m}$  or more, and the opposing electrode is interposed between the liquid crystal and the organic resin film.

*Yokomizu discloses [see Figs. 1 and 2, for instance] an analogous electro-optical device comprising a first substrate [10], a thin film transistor [paragraph 0017] formed over the first substrate, a pixel electrode [13] comprising a first transparent conductive film [paragraph 0018], and electrically connected to the TFT, a second substrate [20] opposed to the first substrate, at least a first colored layer [21B] and a second colored layer [21R] formed on the second substrate wherein the first and second colored layers partly overlap each other to form a light shielding portion [21BM]; an organic resin film [22, paragraph 0021] covering said first and second colored layers and said light shielding portion, an opposing electrode [23] comprising a second transparent conductive film [paragraph 0021], and a liquid crystal [30] interposed between the pixel electrode and the opposing electrode, wherein the organic resin film is interposed between the liquid crystal and the first and second colored layers, and wherein the opposing electrode is interposed between the liquid crystal and the organic resin film. It would have been obvious to one of ordinary skill in the art at the time of the invention to use such an arrangement in the device of Sakamoto, in order to provide a color display, to reduce manufacturing processes by using a overlap of color layers to form a light shielding portion (to block unwanted light leakage), and to provided an organic resin film to flatten the surface (see below) and protect the color layers and opposing electrode from damaging each other.*

*Yokomizu* does not disclose that the organic resin film has a thickness of 1  $\mu\text{m}$  or more; the reference appears to be silent on the thickness of the organic resin film.

*Kanemoto* discloses [see Fig. 1] analogous overlapping color filters, and discloses that the thickness increase where they overlap is 1-2  $\mu\text{m}$  [col. 3, lines 34-36]. *Yoneya* teaches [col. 17, line 65 – col. 18, line 5] that a function of the organic resin film (overcoat layer) is “to flatten a difference in level due to the color filter and the light-shielding film”. It would therefore have been obvious to one of ordinary skill in the art at the time of the invention to make the thickness of the organic resin film large enough to flatten (or at least moderate) a 1-2  $\mu\text{m}$  bump. Doing so requires a thickness of about 1  $\mu\text{m}$  or more, which overlaps the recited range of 1  $\mu\text{m}$  or more; in such cases a *prima facie* case of obviousness exist [see MPEP 2144.05].

Claim 91 is therefore unpatentable.

Regarding the additional limitation of claim 92, that there is a third colored layer in the overlap stack, *Yokomizu* discloses that all three color filters can be stacked to form 21BM [paragraph 0020, for instance], so claim 92 is also unpatentable.

A step (albeit tapered) exists at a portion where the colored layers overlap, so claims 95 and 96 are also unpatentable. The organic resin film is a leveling film, as discussed above with reference to *Yoneya*, so claims 99 and 100 are also unpatentable.

***Allowable Subject Matter***

5. Claims 101 and 102 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. Claims 21-24, 76, 77, 85-90, 93, 94, 97, and 98 are allowed.

7. The following is a statement of reasons for the indication of allowable subject matter:

The prior art does not disclose the electro-optical device of claim 21, in particular the limitations reciting the following electrode structure: a gate electrode and source wiring, a first insulating film formed on them, a semiconductor layer formed over the first insulating film, a second insulating film covering the semiconductor layer, and a gate wiring (connected to gate electrode) and a connection wiring (connecting source wiring to semiconductor layer) formed on the second insulating film. Claim 21 is therefore allowed, as are its dependent claims 22-24, 88-90, 93, and 97.

The prior art does not disclose the electro-optical device of claim 76, in particular the limitations reciting the same electrode structure discussed above with respect to claim 21. Claim 76 is therefore allowed, as are its dependent claims 77, 85-87, 94, and 98.

The prior art does not disclose the electro-optical device of claim 101 or of claim 102, in particular the limitations reciting the following electrode structure: a gate electrode and source wiring, first insulating film formed on them; channel formation, source, and drain regions formed over the first insulating film; a second insulating film

over the channel formation, source, and drain regions; and a gate wiring (connected to gate electrode) and a second wiring (connecting the source wiring to the source region) formed on the second insulating film. Claims 101 and 102 would therefore be allowable if rewritten appropriately.

***Conclusion***

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew Schechter whose telephone number is (571) 272-2302. The examiner can normally be reached on Monday - Friday, 9:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Frank Font can be reached on (571) 272-2415. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Andrew Schechter/  
Primary Examiner, Art Unit 2883  
Technology Center 2800  
24 December 2009